(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 August 2002 (15.08.2002)

PCT

(10) International Publication Number
WO 02/063800 A1

(51) International Patent Classification[7]: H04B 10/00

(21) International Application Number: PCT/US02/03226

(22) International Filing Date: 4 February 2002 (04.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/777,917 5 February 2001 (05.02.2001) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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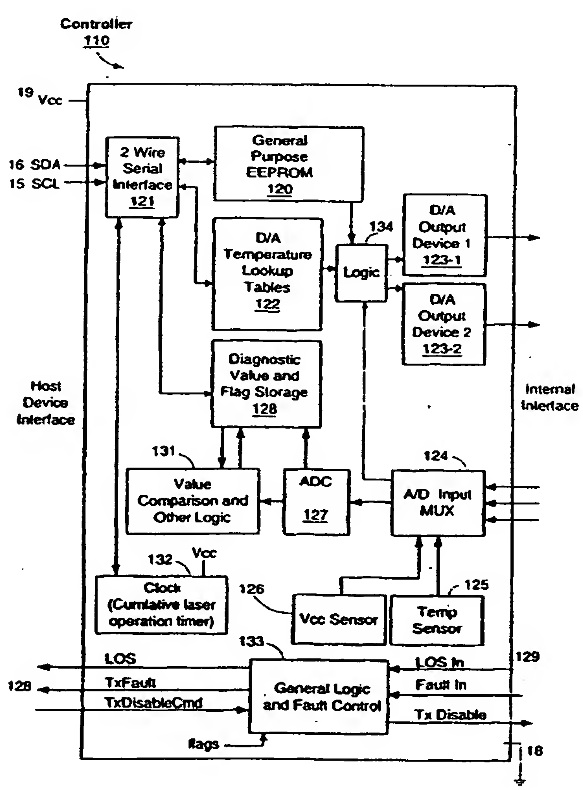
(54) Title: INTEGRATED MEMORY CONTROLLER CIRCUIT FOR FIBER OPTICS TRANSCEIVER



(57) Abstract: A controller (110) for controlling a transceiver having a laser transmitter and a photodiode receiver. The controller includes memory (120, 122, 128) for storing information related to the transceiver, and analog to digital conversion circuitry (127) for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory. Comparison logic (131) compares one or more of these digital values with limit values, generates flag values based on the comparisons, and stores the flag values in predefined locations within the memory. Control circuitry (123-1, 123-2) in the controller controls the operation of the laser transmitter in accordance with one or more values stored in the memory. A serial interface (121) is provided to enable a host device to read from and write to locations within the memory. Excluding a small number of binary input and output signals, all control and monitoring functions of the transceiver are mapped to unique memory mapped locations within the controller. A plurality of the control functions and a plurality of the monitoring functions of the controller are exercised by a host computer by accessing corresponding memory mapped locations within the controller.

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INTEGRATED MEMORY MAPPED CONTROLLER CIRCUIT FOR FIBER OPTICS TRANSCEIVER

The present invention relates generally to the field of fiber optic transceivers and particularly to circuits used within the transceivers to accomplish control, setup, monitoring, and identification operations.

BACKGROUND OF INVENTION

The two most basic electronic circuits within a fiber optic transceiver are the laser driver circuit, which accepts high speed digital data and electrically drives an LED or laser diode to create equivalent optical pulses, and the receiver circuit which takes relatively small signals from an optical detector and amplifies and limits them to create a uniform amplitude digital electronic output. In addition to, and sometimes in conjunction with these basic functions, there are a number of other tasks that must be handled by the transceiver circuitry as well as a number of tasks that may optionally be handled by the transceiver circuit to improve its functionality. These tasks include, but are not necessarily limited to, the following:

- Setup functions. These generally relate to the required adjustments made on a part-to-part basis in the factory to allow for variations in component characteristics such as laser diode threshold current.
- Identification. This refers to general purpose memory, typically EEPROM (electrically erasable and programmable read only memory) or other nonvolatile memory. The memory is preferably accessible using a serial communication standard, that is used to store various information identifying the transceiver type, capability, serial number, and compatibility with various standards. While not standard, it would be desirable to further store in this memory additional information, such as sub-component revisions and factory test data.

implemented using discrete circuitry, for example using a general purpose EEPROM for identification purposes, by inclusion of some functions within the laser driver or receiver circuitry (for example some degree of temperature compensation in a laser driver circuit) or with the use of a commercial micro-controller integrated circuit. However, to date there have not been any transceivers that provide a uniform device architecture that will support all of these functions, as well as additional functions not listed here, in a cost effective manner.

It is the purpose of the present invention to provide a general and flexible integrated circuit that accomplishes all (or any subset) of the above functionality using a straightforward memory mapped architecture and a simple serial communication mechanism.

Fig. 1 shows a schematic representation of the essential features of a typical prior-art fiber optic transceiver. The main circuit 1 contains at a minimum transmit and receiver circuit paths and power 19 and ground connections 18. The receiver circuit typically consists of a Receiver Optical Subassembly (ROSA) 2 which contains a mechanical fiber receptacle as well as a photodiode and pre-amplifier (preamp) circuit. The ROSA is in turn connected to a post-amplifier (postamp) integrated circuit 4, the function of which is to generate a fixed output swing digital signal which is connected to outside circuitry via the RX+ and RX- pins 17. The postamp circuit also often provides a digital output signal known as Signal Detect or Loss of Signal indicating the presence or absence of suitably strong optical input. The Signal Detect output is provided as an output on pin 18. The transmit circuit will typically consist of a Transmitter Optical Subassembly (TOSA), 3 and a laser driver integrated circuit 5. The TOSA contains a mechanical fiber receptacle as well as a laser diode or LED. The laser driver circuit will typically provide AC drive and DC bias current to the laser. The signal inputs for the AC driver are obtained from the TX+ and TX- pins 12. Typically, the laser driver circuitry will require individual factory setup of certain parameters such as the bias current (or output power) level and AC modulation drive to the laser. Typically this is accomplished by adjusting variable resistors or placing factory selected resistors7, 9 (i.e., having factory selected resistance values). Additionally, temperature compensation of the bias current and modulation is often

one or more of these digital values with limit values, generates flag values based on the comparisons, and stores the flag values in predefined locations within the memory. Control circuitry in the controller controls the operation of the laser transmitter in accordance with one or more values stored in the memory. A serial interface is provided to enable a host device to read from and write to locations within the memory. A plurality of the control functions and a plurality of the monitoring functions of the controller are exercised by a host computer by accessing corresponding memory mapped locations within the controller.

In some embodiments the controller further includes a cumulative clock for generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the serial interface.

In some embodiments the controller further includes a power supply voltage sensor that generates a power level signal corresponding to a power supply voltage level of the transceiver. In these embodiments the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory. Further, the comparison logic of the controller may optionally include logic for comparing the digital power level value with a power (i.e., voltage) level limit value, generating a flag value based on the comparison of the digital power level signal with the power level limit value, and storing a power level flag value in a predefined power level flag location within the memory. It is noted that the power supply voltage sensor measures the transceiver voltage supply level, which is distinct from the power level of the received optical signal.

In some embodiments the controller further includes a temperature sensor that generates a temperature signal corresponding to a temperature of the transceiver. In these embodiments the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory. Further, the comparison logic of the controller may optionally include logic for comparing the digital temperature value with a temperature limit value, generating a flag value based on the comparison of the digital temperature signal with the temperature limit value,

invention. It is noted that Memory Map Tables 1, 2, 3 and 4, in addition to showing a memory map of values and control features described in this document, also show a number of parameters and control mechanisms that are outside the scope of this document and thus are not part of the present invention.

The interface 121 is coupled to host device interface input/output lines, typically clock (SCL) and data (SDA) lines, 15 and 16. In the preferred embodiment, the serial interface 121 operates in accordance with the two wire serial interface standard that is also used in the GBIC and SFP standards, however other serial interfaces could equally well be used in alternate embodiments. The two wire serial interface 121 is used for all setup and querying of the controller IC 110, and enables access to the optoelectronic transceiver's control circuitry as a memory mapped device. That is, tables and parameters are set up by writing values to predefined memory locations of one or more nonvolatile memory devices 120, 122, 128 (e.g., EEPROM devices) in the controller, whereas diagnostic and other output and status values are output by reading predetermined memory locations of the same nonvolatile memory devices 120, 121, 122. This technique is consistent with currently defined serial ID functionality of many transceivers where a two wire serial interface is used to read out identification and capability data stored in EEPROM.

It is noted here that some of the memory locations in the memory devices 120, 122, 128 are dual ported, or even triple ported in some instances. That is, while these memory mapped locations can be read and in some cases written via the serial interface 121, they are also directly accessed by other circuitry in the controller 110. For instance, certain "margining" values stored in memory 120 are read and used directly by logic 134 to adjust (i.e., scale upwards or downwards) drive level signals being sent to the D/A output devices 123. Similarly, there are flags stored memory 128 that are (A) written by logic circuit 131, and (B) read directly by logic circuit 133. An example of a memory mapped location not in memory devices but that is effectively dual ported is the output or result register of clock 132. In this case the accumulated time value in the register is readable via the serial interface 121, but is written by circuitry in the clock circuit 132.

implemented in the controller 110 through the use of temperature lookup tables 122 that are used to assign values to the control outputs as a function of the temperature measured by a temperature sensor 125 within the controller IC 110. In alternate embodiments, the controller 110 may use D/A converters with voltage source outputs or may even replace one or more of the D/A converters 123 with digital potentiometers to control the characteristics of the laser driver 105. It should also be noted that while Fig. 2 refers to a system where the laser driver 105 is specifically designed to accept inputs from the controller 110, it is possible to use the controller IC 110 with many other laser driver ICs to control their output characteristics.

In addition to temperature dependent analog output controls, the controller IC may be equipped with a multiplicity of temperature independent (one memory set value) analog outputs. These temperature independent outputs serve numerous functions, but one particularly interesting application is as a fine adjustment to other settings of the laser driver 105 or postamp 104 in order to compensate for process induced variations in the characteristics of those devices. One example of this might be the output swing of the receiver postamp 104. Normally such a parameter would be fixed at design time to a desired value through the use of a set resistor. It often turns out, however, that normal process variations associated with the fabrication of the postamp integrated circuit 104 induce undesirable variations in the resulting output swing with a fixed set resistor. Using the present invention, an analog output of the controller IC 110, produced by an additional D/A converter 123, is used to adjust or compensate the output swing setting at manufacturing setup time on a part-by-part basis.

In addition to the connection from the controller to the laser driver 105, Fig. 2 shows a number of connections from the laser driver 105 to the controller IC 110, as well as similar connections from the ROSA 106 and Postamp 104 to the controller IC 110. These are analog monitoring connections that the controller IC 110 uses to provide diagnostic feedback to the host device via memory mapped locations in the controller IC. The controller IC 110 in the preferred embodiment has a multiplicity of analog inputs. The analog input signals indicate operating conditions of the transceiver and/or receiver circuitry. These analog signals are scanned by a

The limit flags are also sometimes call alarm and warning flags. The host device (or end user) can monitor these flags to determine whether conditions exist that are likely to have caused a transceiver link to fail (alarm flags) or whether conditions exist which predict that a failure is likely to occur soon. Examples of such conditions might be a laser bias current which has fallen to zero, which is indicative of an immediate failure of the transmitter output, or a laser bias current in a constant power mode which exceeds its nominal value by more than 50%, which is an indication of a laser end-of-life condition. Thus, the automatically generated limit flags are useful because they provide a simple pass-fail decision on the transceiver functionality based on internally stored limit values.

In a preferred embodiment, fault control and logic circuit 133 logically OR's the alarm and warning flags, along with the internal LOS (loss of signal) input and Fault Input signals, to produce a binary Transceiver fault (TxFault) signal that is coupled to the host interface, and thus made available to the host device. The host device can be programmed to monitor the TxFault signal, and to respond to an assertion of the TxFault signal by automatically reading all the alarm and warning flags in the transceiver, as well as the corresponding monitored signals, so as to determine the cause of the alarm or warning.

The fault control and logic circuit 133 furthermore conveys a loss of signal (LOS) signal received from the receiver circuit (ROSA, Fig. 2) to the host interface.

Another function of the fault control and logic circuit 133 is to disable the operation of the transmitter (TOSA, Fig. 2) when needed to ensure eye safety. There is a standards defined interaction between the state of the laser driver and the Tx Disable output, which is implemented by the fault control and logic circuit 133. When the logic circuit 133 detects a problem that might result in an eye safety hazard, the laser driver is disabled by activating the Tx Disable signal of the controller. The host device can reset this condition by sending a command signal on the TxDisableCmd line of the host interface.

Yet another function of the fault control and logic circuit 133 is to determine the polarity of its input and output signals in accordance with a set of configuration flags stored in memory 128. For instance, the Loss of Signal (LOS) output of circuit

TABLE 1

MEMORY MAP FOR TRANSCEIVER CONTROLLER

Memory Location (Array 0)	Name of Location	Function
00h - 5Fh	IEEE Data	This memory block is used to store required GBIC data
60h	Temperature MSB	This byte contains the MSB of the 15-bit 2's complement temperature output from the temperature sensor.
61h	Temperature LSB	This byte contains the LSB of the 15-bit 2's complement temperature output from the temperature sensor. (LSB is 0b).
62h - 63h	V_{cc} Value	These bytes contain the MSB (62h) and the LSB (63h) of the measured V_{cc} (15-bit number, with a 0b LSbit)
64h - 65h	B_{in} Value	These bytes contain the MSB (64h) and the LSB (65h) of the measured B_{in} (laser bias current) (15-bit number, with a 0b LSbit)
66h - 67h	P_{in} Value	These bytes contain the MSB (66h) and the LSB (67h) of the measured P_{in} (transmitted laser power) (15-bit number, with a 0b LSbit)
68h - 69h	R_{in} Value	These bytes contain the MSB (68h) and the LSB (69h) of the measured R_{in} (received power) (15-bit number, with a 0b LSbit)
6Ah - 6Dh	Reserved	Reserved
6Eh	IO States	This byte shows the logical value of the I/O pins
6Fh	A/D Updated	Allows the user to verify if an update from the A/D has occurred to the 5 values: temperature, V_{cc}, B_{in}, P_{in} and R_{in}. The user writes the byte to 00h. Once a conversion is complete for a give value, its bit will change to '1'.
70h - 73h	Alarm Flags	These bits reflect the state of the alarms as a conversion updates. High alarm bits are '1' if converted value is greater than corresponding high limit. Low alarm bits are '1' if converted value is less than corresponding low limit. Otherwise, bits are 0b.
74h - 77h	Warning Flags	These bits reflect the state of the warnings as a conversion updates. High warning bits are '1' if converted value is greater than corresponding high limit. Low warning bits are '1' if converted value is less than corresponding low limit. Otherwise, bits are 0b.
78h - 7Ah	Reserved	Reserved

Memory Location (Array 3)	Name of Location	Function of Location
84h - 85h 8Ch - 8Dh 94h - 95h 9Ch - 9Dh A4h - A5h	Temp High Warning V_{cc} High Warning B_{in} High Warning P_{in} High Warning R_{in} High Warning	The value written to this location serves as the high warning limit. Data format is the same as the corresponding value (temperature, V_{cc}, B_{in}, P_{in}, R_{in}).
86h - 87h 8Eh - 8Fh 96h - 97h 9Eh - 9Fh A6h - A7h	Temperature Low Warning V_{cc} Low Warning B_{in} Low Warning P_{in} Low Warning R_{in} Low Warning	The value written to this location serves as the low warning limit. Data format is the same as the corresponding value (temperature, V_{cc}, B_{in}, P_{in}, R_{in}).
A8h - AFh, C5h B0h - B7h, C6h B8h - BFh, C7h	D_{out} control 0-8 F_{out} control 0-8 L_{out} control 0-8	Individual bit locations are defined in Table 4.
C0h	Reserved	Reserved
C1h	Prescale	Selects MCLK divisor for X-delay CLKS.
C2h C3h C4h	D_{out} Delay F_{out} Delay L_{out} Delay	Selects number of prescale clocks
C8h - C9h CAh - CBh CCh - CDh CEh - CFh	V_{cc} - A/D Scale B_{in} - A/D Scale P_{in} - A/D Scale R_{in} - A/D Scale	16 bits of gain adjustment for corresponding A/D conversion values.
D0h	Chip Address	Selects chip address when external pin ASEL is low.
D1h	Margin #2	Finisar Selective Percentage (FSP) for D/A #2
D2h	Margin #1	Finisar Selective Percentage (FSP) for D/A #1
D3h - D6h	PW1 Byte 3 (D3h) MSB PW1 Byte 2 (D4h) PW1 Byte 1 (D5h) PW1 Byte 0 (D6h) LSB	The four bytes are used for password 1 entry. The entered password will determine the Finisar customer's read/write privileges.
D7h	D/A Control	This byte determines if the D/A outputs source or sink current, and it allows for the outputs to be scaled.
D8h - DFh	B_{in} Fast Trip	These bytes define the fast trip comparison over temperature.
E0h - E3h	P_{in} Fast Trip	These bytes define the fast trip comparison over temperature.

TABLE 2 - DETAIL MEMORY DESCRIPTIONS - A/D VALUES AND STATUS BITS

Byte	Bit	Name	Description
Converted analog values. Calibrated 16 bit data.			
96 (60h)	All	Temperature MSB	Signed 2's complement integer temperature (-40 to +125C) Based on internal temperature measurement
97	All	Temperature LSB	Fractional part of temperature (count/256)
98	All	V_{cc} MSB	Internally measured supply voltage in transceiver. Actual voltage is full 16 bit value * 100 uVolt.
99	All	V_{cc} LSB	(Yields range of 0 - 6.55V)
100	All	TX Bias MSB	Measured TX Bias Current in mA Bias current is full 16 bit value *(1/256) mA.
101	All	TX Bias LSB	(Full range of 0 - 256 mA possible with 4 uA resolution)
102	All	TX Power MSB	Measured TX output power in mW. Output is full 16 bit value *(1/2048) mW.
103	All	TX Power LSB	Full range of 0 - 32 mW possible with 0.5 μW resolution, or -33 to +15 dBm)
104	All	RX Power MSB	Measured RX input power in mW RX power is full 16 bit value *(1/16384) mW.
105	All	RX Power LSB	(Full range of 0 - 4 mW possible with 0.06 μW resolution, or -42 to +6 dBm)
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
General Status Bits			
110	7	TX Disable	Digital state of the TX Disable Input Pin
110	6	Reserved	
110	5	Reserved	
110	4	Rate Select	Digital state of the SFP Rate Select Input Pin
110	3	Reserved	
110	2	TX Fault	Digital state of the TX Fault Output Pin
110	1	LOS	Digital state of the LOS Output Pin
110	0	Power-On-Logic	Indicates transceiver has achieved power up and data valid
111	7	Temp A/D Valid	Indicates A/D value in Bytes 96/97 is valid
111	6	V_{cc} A/D Valid	Indicates A/D value in Bytes 98/99 is valid

TABLE 3 - DETAIL MEMORY DESCRIPTIONS - ALARM AND WARNING FLAG BITS

Byte	Bit	Name	Description
Alarm and Warning Flag Bits			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
112	5	V_{cc} High Alarm	Set when internal supply voltage exceeds high alarm level.
112	4	V_{cc} Low Alarm	Set when internal supply voltage is below low alarm level.
112	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
112	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
112	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
112	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
113	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
113	5-0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
116	6	Temp Low Warning	Set when internal temperature is below low warning level.
116	5	V_{cc} High Warning	Set when internal supply voltage exceeds high warning level.
116	4	V_{cc} Low Warning	Set when internal supply voltage is below low warning level.
116	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
116	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
116	1	TX Power High Warning	Set when TX output power exceeds high warning level.
116	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.

TABLE 4

Byte Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X-out cntl0	T alrm hi set	T alrm lo set	V alrm hi set	V alrm lo set	B alrm hi set	B alrm lo set	p alrm hi set	P alrm lo set
X-out cntl1	R alrm hi set	R alrm lo set	B ft hi set	P ft hi set	R ft hi set	D-in inv set	D-in set	F-in inv set
X-out cntl2	F-in set	L-in inv set	L-in set	Aux inv set	Aux set	T alrm hi hib	T alrm lo hib	V alrm hi hib
X-out cntl3	V alrm lo hib	B alrm hi hib	B alrm lo hib	P alrm hi hib	P alrm lo hib	R alrm hi hib	R alrm lo hib	B ft hi hib
X-out cntl4	P ft hi hib	R ft hi hib	D-in inv hib	D-in hib	F-in inv hib	F-in hib	L-in inv hib	L-in hib
X-out cntl5	Aux inv hib	Aux hib	T alrm hi clr	T alrm lo clr	V alrm hi clr	V alrm lo clr	B alrm hi clr	B alrm lo clr
X-out cntl6	P alrm hi clr	P alrm lo clr	R alrm hi clr	R alrm lo clr	B ft hi clr	P ft hi clr	R ft hi clr	D-in inv clr
X-out cntl7	D-in clr	F-in inv clr	F-in clr	L-in inv clr	L-in clr	Aux inv clr	Aux clr	EE
X-out cntl8	latch select	invert	o-ride data	o-ride select	S reset data	HI enable	LO enable	Pullup enable
Prescale	*reserved*	*reserved*	*Reserved*	*reserved*	B^3	B^2	B^1	B^0
X-out delay	B^7	B^6	B^5	B^4	B^3	B^2	B^1	B^0
chip address	b^7	b^6	b^5	b^4	b^3	b^2	b^1	x
X-ad scale MSB	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
X-ad scale LSB	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
D/A cntl	source/ sink	D/A #2 range			source/sink	D/A #1 range		
	1/0	2^2	2^1	2^0	1/0	2^2	2^1	2^0
config/O-ride	manual D/A	manual index	manual AD alarm	EE Bar	SW-POR	A/D Enable	Manual fast alarm	*reserved*
Internal State 1	D-set	D-inhibit	D-delay	D-clear	F-set	F-inhibit	F-delay	F-clear
Internal State 0	L-set	L-inhibit	L-delay	L-clear	*reserved*	*reserved*	*reserved*	*reserved*
I/O States 1	*reserved*	F-in	L-in	*reserved*	D-out	*reserved*	*reserved*	*reserved*
Margin #1	Reserved	Neg_Scale 2	Neg_Scale 1	Neg_Scale 0	Reserved	Pos_Scale 2	Pos_Scale 1	Pos_Scale0
Margin #2	Reserved	Neg_Scale 2	Neg_Scale 1	Neg_Scale 0	Reserved	Pos_Scale 2	Pos_Scale 1	Pos_Scale0

4. The single-chip integrated circuit of claim 3, wherein
the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

5. The single-chip integrated circuit of claim 1, further including:
a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

6. The single-chip integrated circuit of claim 5, wherein
the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

7. The single-chip integrated circuit of claim 1, further including
fault handling logic, coupled to the transceiver for receiving at least one fault signal from the transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate the computed fault signal.

8. A single-chip integrated circuit for controlling an optoelectronic device, comprising:

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

comparing the digital values with limit values, generating flag values based on the limit values, and storing the flag values in predefined locations within the memory;

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory.

11. The method of claim 10, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via the memory interface.

12. The method of claim 10, further including:

converting an analog power supply voltage level signal, corresponding to a voltage level of the transceiver, into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

13. The method integrated circuit of claim 12, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

14. The method of claim 10, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

comparing the digital values with limit values, generating flag values based on the limit values, and storing the flag values in predefined memory mapped locations within the controller;

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the predefined memory mapped locations within the controller;

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the controller.

19. The method of claim 18, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a memory mapped within the controller.

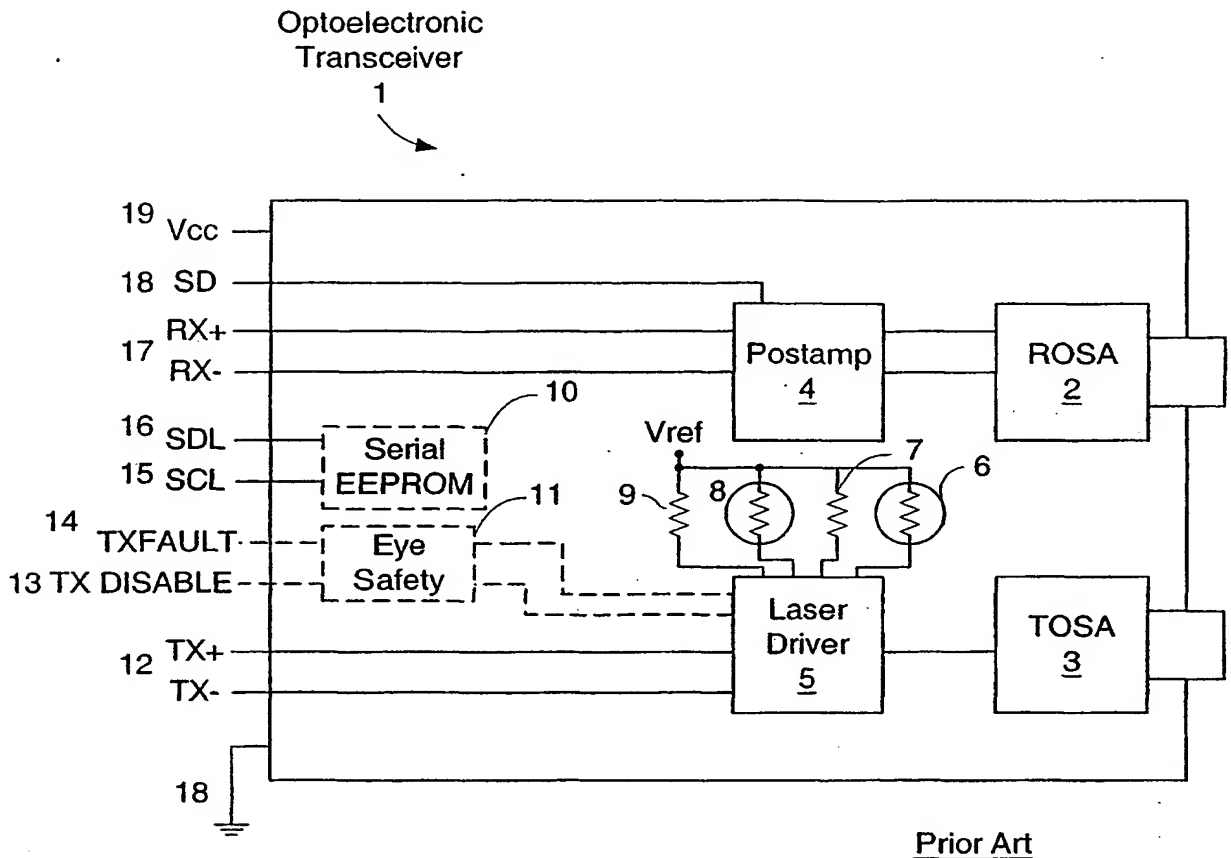
Optoelectronic
Transceiver
1
19 Vcc
18 SD
RX+
17
RX-
16 SDL
15 SCL
14
TXFAULT
13 TX DISABLE
TX+
12
TX-
18
10
Serial
EEPROM
11
Eye
Safety
Vref
9
8
7
6
Postamp
4
ROSA
2
Laser
Driver
5
TOSA
3
Prior Art

Fig. 1

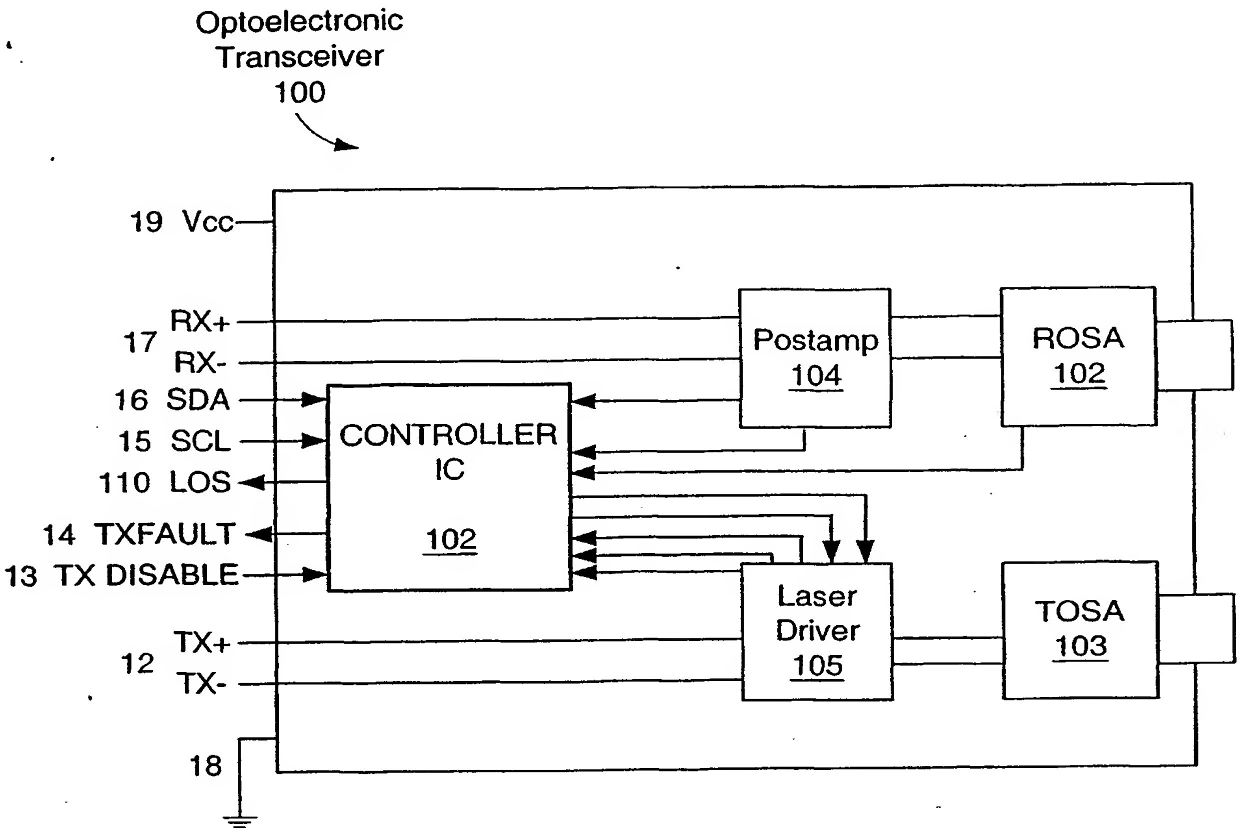
Optoelectronic
Transceiver
100
19 Vcc
17
RX+
RX-
16 SDA
15 SCL
110 LOS
14 TXFAULT
13 TX DISABLE
12
TX+
TX-
18
CONTROLLER
IC
102
Postamp
104
ROSA
102
Laser
Driver
105
TOSA
103

Fig. 2

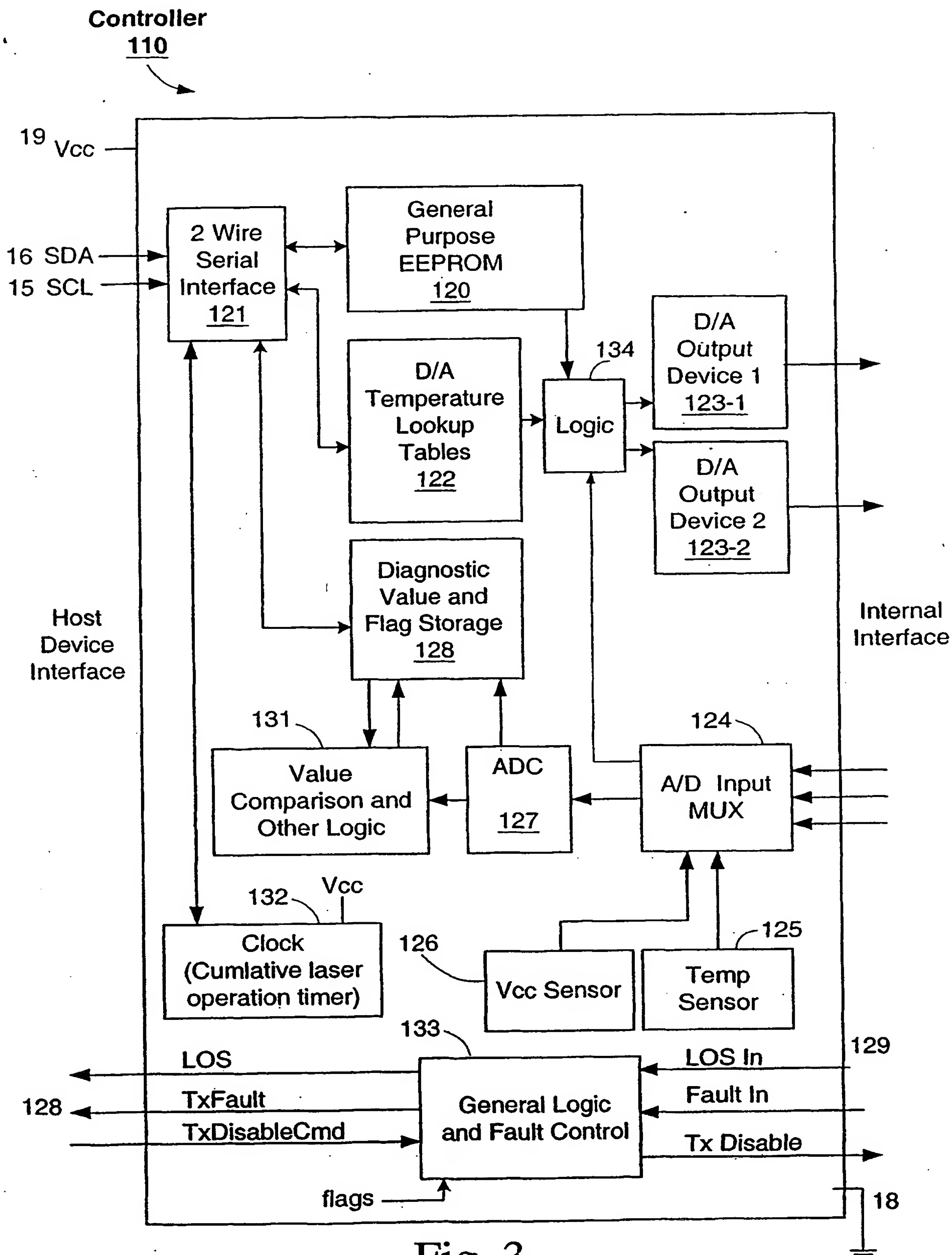
Controller
110
19 Vcc
16 SDA
15 SCL
2 Wire Serial Interface 121
General Purpose EEPROM 120
D/A Temperature Lookup Tables 122
134
Logic
D/A Output Device 1 123-1
D/A Output Device 2 123-2
Diagnostic Value and Flag Storage 128
Host Device Interface
Internal Interface
131
Value Comparison and Other Logic
ADC 127
124
A/D Input MUX
132
Vcc
Clock (Cumlative laser operation timer)
126
Vcc Sensor
125
Temp Sensor
133
General Logic and Fault Control
LOS
TxFault
TxDisableCmd
128
LOS In
Fault In
Tx Disable
129
flags
18

Fig. 3